Remarks

This Amendment is responsive to the **December 12, 2007** Office Action. Reexamination and reconsideration of **claims 1-23** is respectfully requested.

Summary of The Office Action

The Title was objected to as being not descriptive.

The specification was objected to for not capitalizing trademarks used in the application.

Claims 1-4, 6-8, 10-12, 16-20, 22 and 23 were rejected under 35 U.S.C. §103(a) as purportedly being unpatentable over Shishizuka (US Patent No. 6,697,898 B1) (Shishizuka) in view of Westervelt (US Patent Appl. 2003/0231330 A1) (Westervelt).

Claims 5, 9, 13, 14, 15 and 21 were rejected under 35 U.S.C. §103(a) as purportedly being unpatentable over Shishizuka, in view of Westervelt, in view of well-known prior art.

The Present Amendment

The Title has been amended to include the suggestions of the Office Action to include the word "parallel."

Paragraphs [0016] and [0028] have been amended to reflect the changes suggested in the Office Action regarding the use of the trademark FIREWIRE.

Dependent claim 2 has been amended. The subject matter is supported by, for example, paragraph [0026] on page 7 of the specification and Figure 1. Thus, no new matter has been added.

I. Claims 1-4, 6-8, 10-12, 16-20, 22 and 23 were rejected under 35 U.S.C. §103(a) as being unpatentable over Shishizuka in view of Westervelt.

To establish a prima facie case of 35 U.S.C. §103 obviousness the prior art reference (or references when combined) must teach or suggest all the claim limitations. MPEP 2143.03. Furthermore under MPEP 2131 for a reference to anticipate a claim, "[t]he elements must be arranged as required by the claim, but this is not an *ipsissimis verbis* test, i.e., identity of terminology is not required. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990)."

As explained in the following, the references fail to teach or suggest all claim elements. Furthermore, the components relied upon by the Office Action from Shishizuka and Westervelt are not arranged as required by the claims. Therefore, a prima facie obviousness rejection is not established by the combined references.

Independent Claim 1

Claim 1 recites an image forming device comprising a scanner, a memory, a page frame buffer, an imaging mechanism, and a dual bus system with a specific configuration. Shishizuka fails to teach or suggest the claimed image forming device and dual bus system as alleged by the Office Action.

Claim 1 recites the dual bus system as:

> "a dual bus system configured to allow parallel transmission of data where the image data can be transmitted from the scanner to the memory simultaneously with transmitting the page of data from the page frame buffer to the imaging mechanism."

As recited, there are two data transmission paths formed by the dual bus system: one bus is connected so that image data is transmitted (1) from the scanner to the memory, and another bus allows simultaneously transmitting the page of data (2) from the page frame buffer to the imaging mechanism. This arrangement of elements and configuration of the dual bus is not taught or suggested by references.

The Office Action cites the "DoEngine" of Shishizuka as teaching the claimed dual bus system. Within the DoEngine (which is best seen in Figure 4), the Office Action cites the two buses, the G bus 404 and the B bus 405. (Office Action, page 5, lines 5-8). However, the DoEngine fails to teach the claimed configuration. The G bus 404 transmits data between the scanner controller 4302 to the cache memory 403 (via system bus bridge 402), and the B bus transmits data from the cache memory 403 to the printer controller 4303 (via system bus bridge 402). A page frame buffer (being a separate element from the cache memory 403) is not present and not part of the G bus and B bus configuration. Thus, the claimed page frame buffer and the claimed arrangement with the recited dual bus system is not taught by the G and B buses of Shishizuka.

The Office Action then cites different bus components from Shishizuka as being a first and second bus that teach the claimed dual bus system (OA, page 6 last paragraph). In particular, the Office Action states:

> Therefore, SHISHIZUKA teaches a first bus (i.e., from the interface "VIDEO I/F TO SCANNER" to the "Scanner Controller" 4302 to either of the G bus or B bus (by means of a "G Bus/B Bus I/F" 4301A) which are connected to SDRAM by means of a "System Bus Bridge" 402, "MC Bus", "SDRAM & ROM Controller (MC)" 403, and "Memory BUS", all shown in Fig. 4) which connects the "scanner to the memory" and
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> a second bus (i.e., from the "Printer Controller" 4303 containing the printer controller FIFO to the printer and is shown as "VIDEO I/F TO PRINTER" in Fig. 4) which connects the "page frame buffer to the imaging mechanism". Data can be transmitted from the scanner to memory while simultaneously transmitting data from the page frame buffer to the printer.]
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> (OA, page 6 last paragraph)

Applicant notes that the "I/F" elements referred to by Shishizuka are interface ports, not a bus (Shishizuka, col. 35, lines 54-56: "The scanner device I/F is an input/output port..."). Thus the first and second buses explained by the Office Action comprise multiple components connected by interface ports (e.g. I/F) and multiple communication paths, none of which teaches the dual bus that can transmit image data from the scanner to the memory simultaneously with transmitting the page of data from the page frame buffer to the imaging mechanism. Looking more closely to the components involved, figure 45 of Shishizuka discloses the scanner video I/F connections and components, and figures 66-67 disclose the printer controller 4303 components and connections including the printer device I/F. The multiple components involved and multiple communication channels therebetween are shown to pass different signals between each other over the different communication channels. Thus the multiple channels and paths relied upon by the examiner cannot constitute a first or second bus, and fail to teach or suggest a first bus and a second bus as proposed by the Office Action.

Additionally, the conclusion made by the examiner in the last sentence from the cited text above, that "[d]ata can be transmitted from the scanner to memory while simultaneously transmitting data from the page frame buffer to the printer" is not supported by Shishizuka and no citation to an actual teaching in Shishizuka is provided (OA, page 6 last paragraph). Accordingly, Shishizuka fails to teach or suggest the elements relied upon by the rejection.

The Office Action identifies a deficiency in Shishizuka as not teaching a page frame buffer configured to store a page of data and cites Westervelt's first-in-first-out FIFO buffer 353 to cure the deficiency (Office Action, page 7). The combination still fails to teach or suggest the claimed elements because simply adding a FIFO buffer to Shishizuka does not cure the fact that the claimed dual bus and the claimed arrangement of components is not taught by Shishizuka. Furthermore, Westervelt fails to teach or suggest how its FIFO buffer would be connected and where it would be connected into the DoEngine of Shishizuka. Indeed, the DoEngine already includes a cache memory 403 (figure 4) and the printer controller 4303 already includes a FIFO buffer 6608 (figure 66). One of ordinary skill in the art would have no reason to add another buffer to the DoEngine of Shishizuka. Adding a buffer would increase cost, further complicate the circuit, and require reconfiguration of the components. Thus the motivation to combine provided by the Office Action (page 7, 3rd parag.) is not supported by the references. Rather, the combination is made using impermissible hindsight using the claims as a blueprint. The rejection is improper.

Accordingly, a prima facie obviousness rejection has not been established. Claim 1 patently distinguishes over the references of record and should now be allowed. As such, dependent claims 2-10 are also not obvious and should now be allowed.

Shishizuka's VSYNC and HSYNC Timing Signals

The Office action relies upon Shishizuka's discussion of vertical synchronous signals (VSYNC) to the printer, horizontal synchronous signals (HSYNC), and a video clock (Office Action, pages 5-6). Applicant respectfully submits the VSYNC and HSYNC signals are not relevant to the claim language. These timing signals and how they are processes fail to teach or suggest simultaneous or parallel transmission of data by a dual bus transferring data from page frame memory to the imaging mechanism while also transferring image data from a scanner to main memory. Thus, this cited section of Shishizuka is not on point and fails to support the rejection.

Dependent Claim 2

Claim 2 recites that the dual bus system includes a first bus connected to communicate data between the scanner and the memory, and a second bus, independent from the first bus, connected to communicate data between the page frame memory and the imaging mechanism. The office action relies on Shishizuka based on the alleged first and second buses as asserted under claim 1 (Office Action, bottom of page 7-8. As explained above, no such first or second bus is taught or suggested. Thus the rejection of claim 2 is improper and should be withdrawn.

Independent Claim 11

The Office Action on page 12 states that the recited claim language "transmitting the first image data page for imaging to an imaging mechanism where the transmitting occurs in parallel with the loading" is taught by Shishizuka as follows:

> Simultaneously, the printer controller (PRC) outputs the vertical synchronous signal (VSYNC) to the printer. Thereafter, the horizontal synchronous signal (HSYNC) and the video clock are input from the printer. In synchronization with the HSYNC and the video clock, the printer controller outputs the image data from the internal FIFO to the printer. (Shishizuka , col. 66, lines 62-67)

Applicant respectfully submits that the cited text teaches outputting image data from the printer controller in synchronization with the HSYNC and VSYNC timing signals. The timing signals are not image data pages that are generated from scanning sheets of print media as recited in the claim, and the timing signals are not image data pages loaded into a memory.

As such, the VSYNC and HSYNC timing signals, as well as the processing of the timing signals, are irrelevant to the claimed elements. Thus, the cited text fails to teach or suggest "transmitting the first image data page for imaging to an imaging mechanism where the transmitting occurs in parallel with the loading" as recited in claim 11. Accordingly, Shishizuka fails to teach or suggest the elements relied upon by the rejection and fails to support a prima facie rejection.

Furthermore, the Office Action relies on Westervelt for teaching the element of copying a page into a page frame memory. In view of the deficiencies of Westervelt and the deficiencies in combining Westervelt and Shishizuka as explained under claim 1, Westervelt fails to cure the deficiencies of Shishizuka.

Therefore the combined references still fail to establish a prima facie obviousness rejection. The rejection is improper and should be withdrawn. Claim 11 should now be allowed. Accordingly, the rejection of dependent claims 12-16 are also improper and should be withdrawn. All claims are now in condition for allowance.

Independent Claim 17

Claim 17 was rejected based on similar reasoning as applied against claim 1 (Office Action, starting on page 15). As explained under claim 1, the examiner's reliance on Shishizuka is not on point and does not teach the bus structure as claimed. Thus, Shishizuka fails to teach or suggest the recited arrangement of a first data bus, a second data bus, and parallel transmission of data between components as recited in claim 17.

Furthermore, the Office Action's reliance on Westervelt for teaching a FIFO buffer is not sufficient to cure the deficiencies of Shishizuka. As explained under claim 1, the combined references still fail to establish a prima facie obviousness rejection. The rejection is improper and should be withdrawn. Claim 17 should now be allowed. Accordingly, the rejection of dependent claims 18-23 are also improper and should be withdrawn. All claims are now in condition for allowance.

II. Claims 5, 9, 13, 14, 15 and 21 were rejected under 35 U.S.C. §103(a) as being unpatentable over Shishizuka in view of Westervelt in view of well known prior art.

Claims 5, 9, 13, 14, 15 and 21 are dependent claims. Since the rejection of their respective independent claims has been shown to be unsupported and improper, then the rejection of the dependent claims is also improper. Shishizuka and Westervelt fail to establish a prima facia obviousness rejection of any claim. The deficiencies are not cured by what is alleged to be well known prior art. Thus prima facie obviousness rejection is not established by the references and the rejection is improper. The rejection should be withdrawn and all claims allowed.

Conclusion

For the reasons set forth above, claims 1-23 patentably and unobviously distinguish over the references and are allowable. An early allowance of all claims is earnestly solicited.

Respectfully submitted,

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